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Horizontally aligned ZnO nanowire transistors using patterned graphene thin films

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Here we report the directed growth of ZnO nanowires on multilayer graphene films (MGFs) without the use of metal seed materials. The ZnO source substance was diffused onto the MGF surface, where nanowires tended to grow in the high surface energy sites. This property was exploited to fabricate top-gate structural nanowire transistors with ZnO nanowires grown in the direction of the exposed sides of $6 \times 4 \mu\text{m}$ patterned MGFs with a SiO₂ capping layer. The devices showed an on-current of 160 nA, a threshold voltage of -2.27 V , an on-off current ratio of 3.98×10^5 , and a field effect mobility of $\sim 41.32 \text{ cm}^2/\text{V}\cdot\text{s}$. © 2012 American Institute of Physics. [doi:10.1063/1.3684614]

A graphene thin film (GTF) with a unique two-dimensional crystal structure has outstanding conductivity, flexibility, and transparency despite its thinness. These desirable characteristics have made GTFs the focus of intense research and given them the potential for numerous materials applications.^{1,2} It is expected that GTFs will be commonly used for the metal electrode in various consumer products as well as the electrode material for the next generation of transparent, flexible displays due to their remarkable conductivity.^{3,4} The utility of GTFs is not limited to electronics, and they have found applications in such diverse fields as environmental science and bio-devices; they can also serve as gas sensors because they react to specific gases such as CO_x and NO_x.^{5,6}

Similarly, nanowires have also recently attracted much attention owing to their usefulness in fabricating highly integrated electronic devices, and various semiconducting nanowires are currently being investigated for this purpose.^{7,8} However, well-operated production of such devices depends greatly on the ability to control the alignment of nanowires at specific locations, which often proves to be problematic. The most commonly used method for nanowire placement requires growing nanowires on a massive scale and then dispersing them on the substrate where devices will be produced. This method is easy, as the methods for growing and dispersing nanowires are widely known, but it is less effective at aligning nanowires at desired locations and often results in poor placement of nanowires and malfunction of the device.

However, there is a second method for nanowire placement that involves growing the nanowires directly on the substrate, which provides effective alignment, but there are no established techniques to accomplish this even though numerous research groups are pursuing its development. This second method can be divided into two approaches: top-down and bottom-up. The top-down approach involves etching a single crystal silicon wafer until nanoscale features

corresponding to nanowires are obtained, which can be achieved through control of the etching time with high-resolution e-beam lithography or existing lithography techniques.^{9–11} However, the top-down approach is not compatible with all materials. The bottom-up approach involves the use of seed materials to guide the growth of nanowires directly on the substrate. In principle, this approach is compatible with a wide range of materials but has attained only limited achievement thus far.

In this context, the combination of graphene films and nanowires, two next-generation materials, promises to fill the need for bottom-up fabrication of nanowire devices. The fabrication of graphene devices taking advantage of the size of nanowire electrodes and masks has been reported, as well as the use of graphene and nanowire transistors in a high-frequency circuit.^{12–14}

In the current work, we demonstrate the growth of nanowires on graphene films via chemical vapor deposition (CVD), and we have characterized the ZnO nanowires using x-ray diffraction and room temperature photoluminescence. Moreover, we fabricated an aligned nanowire transistor by employing multilayer graphene films (MGFs) as a catalyst for growing ZnO nanowires, and we examined transistor characteristics.

Nickel foil (Nilaco, 0.1 mm thick) was placed in a quartz tube (2 in. diameter) of a conventional thermal chemical vapor deposition (TCVD) system. In order to clean the surface and eliminate the thin surface oxide layer, the sample was heated to 900 °C under H₂ flow of 100 sccm for 30 min. Acetylene (C₂H₂) as a precursor for graphene growth was then introduced into the quartz tube with a flow rate of 5 sccm for 3 min, and then the sample was cooled slowly down to room temperature with H₂ flowed at 100 sccm. Poly-methyl methacrylate (PMMA) was used to transfer the MGF from Ni onto silicon wafer substrate. The underlying Ni was etched by a commercial Ni etchant (Type 1 from Transene Company) and PMMA was removed by acetone.

The number of graphene layers and the quality of transferred graphene were assessed using micro-Raman spectroscopy (Renishaw RM1000-Invia) with an excitation

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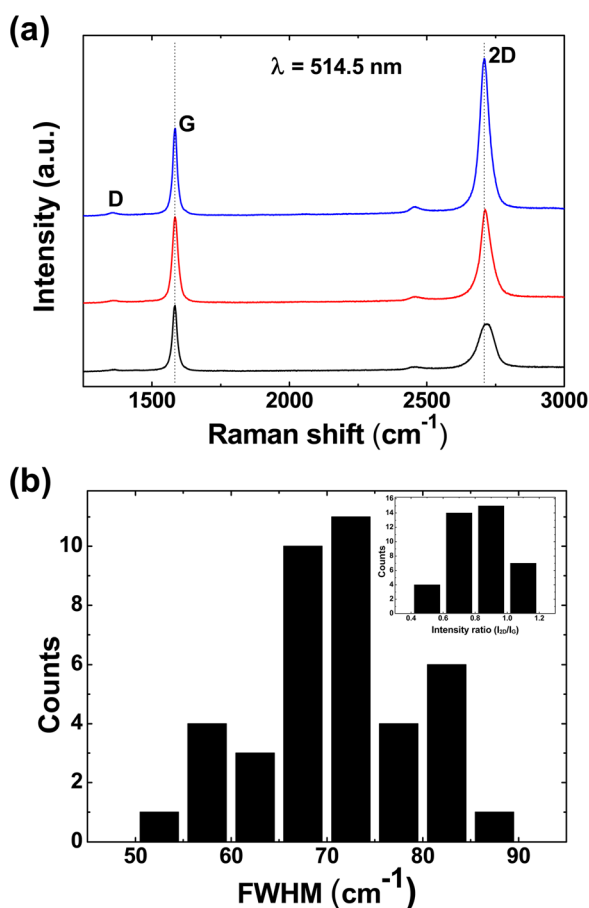


FIG. 1. (Color online) (a) Raman spectrum of a MGF. (b) Distribution of full width at half maximum (FWHM) and intensity ratio (I_{2D}/I_G) of 40 points on MGFs.

wavelength of 514.5 nm (2.41 eV). The Raman spectra exhibit three major features (Fig. 1(a)). The G ($\sim 1580 \text{ cm}^{-1}$) and 2D ($\sim 2700 \text{ cm}^{-1}$) peaks originate from the in-plane vibration of sp^2 carbon atoms and two phonon double resonance Raman processes, respectively, while the D ($\sim 1350 \text{ cm}^{-1}$) peak originates from defects.^{15,16} The strongly suppressed D peak in Fig. 1(a) indicates high-quality graphene, and the relative intensity ratio between the 2D and G peaks ($I_{2D}/I_G > 0.5$) shows that our MGF sample consists of only a few layers.^{17,18} In order to examine the thickness distributions of the graphene, Raman spectroscopy was conducted and the full width at half maximum (FWHM) at each point and the intensity ratio (I_{2D}/I_G) between the 2D peak and the G peak were measured (Fig. 1(b)). The I_{2D}/I_G and the FWHM in the monolayer graphene, the bilayer graphene, and trilayer graphene are known to be >2 and ~ 30 , 1.0-2.0 and ~ 46 , and 0.75-1.0 and ~ 70 , respectively.^{19,20} As shown in Fig. 1(b), the thickness at 17 points among 40 points on the fabricated MGF was below 70, indicating a trilayer structure, whereas the thickness at the rest of the points was larger and suggested the presence of four or more layers.

The substrate bearing the transferred MGF and the ZnO source material were placed on each side of the CVD chamber, and the temperatures were increased to 750°C and 1070°C to facilitate the growth of ZnO nanowires. Figure 2(a) shows the field-emission scanning electron microscopy

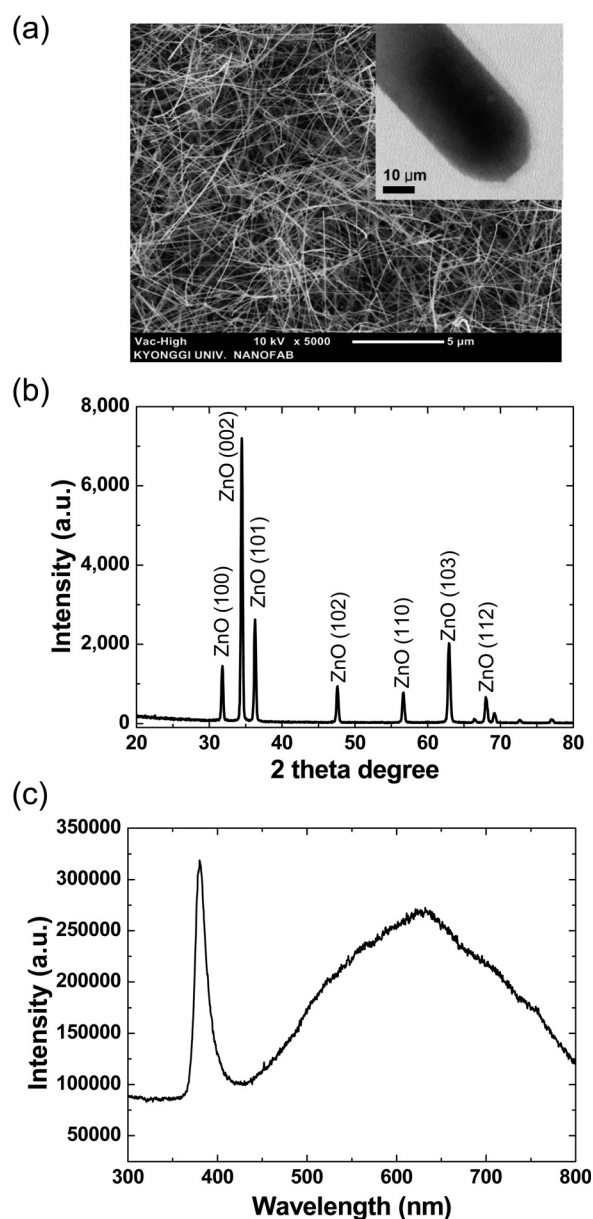


FIG. 2. ZnO nanowires grown on MGFs. (a) FE-SEM image and the inset of HR-TEM image. (b) XRD spectrum. (c) Room-temperature PL spectrum.

(FE-SEM) image of the sample, which reveals that the ZnO nanowires grew very densely on the MGF substrate. Their diameter and length were measured and found to be over ~ 30 nm and $\sim 5 \mu\text{m}$, respectively. The inset of Fig. 2(a) shows the high resolution transmission electron microscope (HR-TEM) of typical tip of a ZnO nanowire. It confirms that the top area does not show evidence for metal seeds. Moreover, it was proved that ZnO nanowires were uniformly grown on graphene thin films with different thicknesses (2-20 layers). Figure 2(b) shows the results from x-ray diffraction (XRD) analysis to determine the crystal structure of the ZnO nanowires, which corresponds to a wurtzite hexagonal structure with lattice constants $a = 3.2535$ and $c = 5.2151$ (ICDD No. 80-0074). The most dominant peak in the XRD spectrum of the ZnO nanowires is (002), indicating that the nanowires were oriented about the c -axis.^{21,22} Figure 2(c) shows the result of room temperature photoluminescence (PL) analysis, in which the near-band-edge emission and the

secondary peak are observed at around 380 and 630 nm, respectively. While the origin of this longer wavelength peak has not been clearly identified, the peak was shown to be closely associated with surface defects arising in the course of growing ZnO nanowires.^{23–25}

The growth mechanism of ZnO nanowires on MGFs is not entirely understood, although there are some plausible hypotheses. Zinc, which has a low melting point among ZnO nanowire components, may form a catalytic droplet on the MGFs which promotes the growth of nanowires.²⁶ Moreover, it is possible that the ZnO source substance diffuses onto the surface of the MGFs, and nanowires grow in the high surface energy sites of this layer.²⁷ As shown HR-TEM image of Fig. 1(a), we confirmed the absence of metal seed drop on the tip of ZnO nanowires on MGFs. Therefore we put more weight on the latter growth mechanism. Control of the location and orientation of the nanowires can be accomplished without the use of metal seeds by growing the nanowires on the exposed sides of MGFs. Graphene can be patterned relatively easily through O₂ plasma etching, which enables ZnO nanowires to be grown only in the remaining MGFs areas after etching where transistors will be fabricated. This hybrid structure offers a solution to the problems associated with nanowire alignment at desired locations in the fabrication of nanowire devices, which we chose to pursue.

It is important to emphasize that this mechanism is distinct from that by which nanowires are grown using metal seed materials, in which the Au seed is found at the tip of each nanowire. If nanowires are grown through the use of Au seeds and subsequently transferred to another substrate, problems may arise from the presence of the metal seed left at the tip of each nanowire. In particular, Au is known to develop unwanted deep levels in semiconductors including Si.^{26,28} To date, there have been no quantitative analyses of the effects of the residual metal seed on nanowire performance, which are considered to retain high reactivity in the fabrication of electronic, electrical, optical, and chemical devices after growth of the nanowires has been accomplished. However, such effects are irrelevant to ZnO nanowires grown on the MGFs as demonstrated in this study, as metal seed materials are not used and there are no residual metals left on the nanowires that may affect their performance. In addition to the current work, several other studies have verified that nanowires can be grown by methods that do not employ the use of a metal seed, utilizing materials such as Si, ZnO, and InAs.^{26,29,30}

Figure 3(a) shows the schematic diagram of a nanowire transistor made using nanowires grown via the method we report here. First, a MGF sample was grown and transferred onto a substrate consisting of a silicon wafer on which SiO₂ was thermally grown. The MGF was then used as a substrate for the fabrication of a top-gate structural nanowire transistor. A research result has been reported that ZnO nanostructures were vertically grown on graphene layers.³¹ However, vertical growth of nanowire should be prevented in order to conduct post process following nanowire growth during the fabrication of nanowire transistor devices using the conventional photolithography. We proved through several rounds of experiment that ZnO nanowires were not able to grow

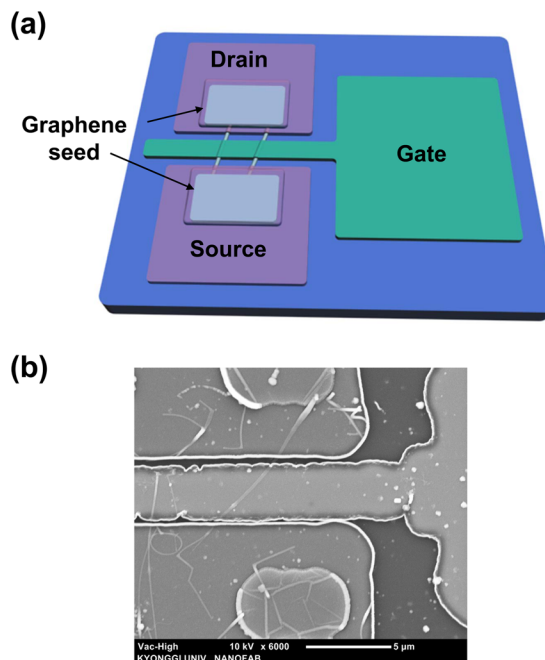


FIG. 3. (Color online) (a) Schematic diagram of the top-gate structural ZnO nanowire transistor. (b) FE-SEM image of ZnO nanowire transistor fabricated on MGF. Scale bar = 5 μm .

through SiO₂ thin film to a vertical direction in case SiO₂ layer with over ~ 70 nm of thickness was covered on top of the MGFs. Thus, 100 nm-thick patterned SiO₂ thin film ($6 \mu\text{m} \times 4 \mu\text{m}$) was formed as a capping layer onto the MGFs. The MGF areas, which were not covered with SiO₂ capping layer, were then removed through O₂ plasma etching process. As a result, only the MGF with SiO₂ capping layer ($6 \mu\text{m} \times 4 \mu\text{m}$) was left on the substrate. This structure has an advantage that nanowires can grow horizontally with substrates and be used as transistor channels because only the side of MGF is exposed. Consequently, this method allows the horizontal nanowire alignment, which is expected to be applied to the fabrication of devices with high yield rates.

ZnO nanowire was grown using the exposed edge of the MGF under the SiO₂ layer as a catalyst through CVD. Both ends of the nanowire were sputtered with a double metal layer consisting of 70 nm aluminum and 50 nm indium tin oxide (ITO) to form a source-drain electrode. The entire substrate was covered with 30 nm Al₂O₃ by atomic layer deposition (ALD), which was used as a gate insulating layer. In order to form a hole to the source-drain electrode so that voltage could be applied to it, a contact hole pattern was formed by photoresist and was etched using buffered oxide etch (BOE) solution. Finally, a top gate electrode was formed by sputtering 70 nm Al and 50 nm ITO on top of the transistor. The FE-SEM image in Fig. 3(b) reveals that the graphene and nanowires grown from the catalyst are located at the lower part of source-drain electrode in the fabricated top-gate nanowire transistor. By employing this fabrication process, nanowires were grown at desired locations and the transistor was fabricated using the nanowires as a channel.

The electrical characteristics of the ZnO nanowire transistor grown on MGF are shown in Fig. 4. The drain current versus gate-source voltage ($I_{\text{ds}}-V_{\text{gs}}$) and drain current versus drain-source voltage ($I_{\text{ds}}-V_{\text{ds}}$) of a representative device are

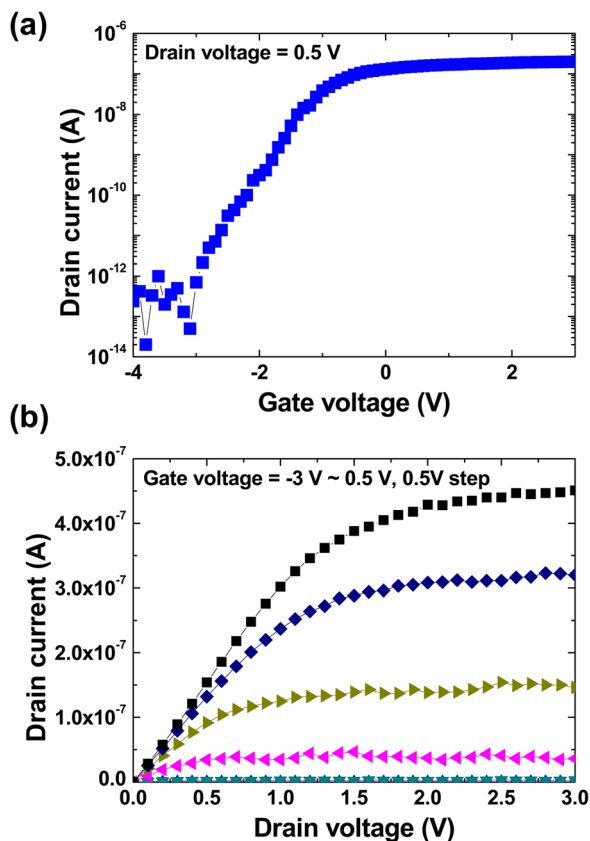


FIG. 4. (Color online) (a) Drain-current versus gate-source voltage (I_{ds} - V_{gs}) properties at $V_{ds}=0.5$ V for representative ZnO nanowire transistors. (b) Drain-current versus drain-source voltage (I_{ds} - V_{ds}) properties for representative ZnO nanowire transistors.

displayed in Figs. 4(a) and 4(b), respectively. ZnO nanowires grown on MGFs exhibit the typical characteristics of an n-type semiconductor transistor (Fig. 4). Parameters such as threshold voltage (V_{th} , V_{gs} at $I_{ds}=0.1$ nA, $V_{ds}=0.5$ V), on-current (I_{on} , I_{ds} at $V_{gs}=V_{th}+3$ V, $V_{ds}=0.5$ V), and sub-threshold slope (SS, the difference between V_{gs} at $I_{ds}=1$ nA and V_{gs} at $I_{ds}=0.1$ nA) evaluated from the V_{gs} - I_{ds} curve in Fig. 4(a) are -2.27 V, 160 nA, and 0.43 V/dec, respectively. The on-off current ratio (I_{on}/I_{off}), a parameter indicating the switching properties of devices, is 3.98×10^5 . Moreover, the field effect mobility was evaluated through a gate-channel capacitance model ($C_i = 2\pi\epsilon_0\epsilon_{eff}L/\cosh^{-1}(1+t_{ox}/r)$) and a metal-oxide semiconductor field-effect transistor (MOSFET) model ($\mu = dI_{ds}/dV_{gs} \times L^2/C_i \times 1/V_s$).³²⁻³⁶ The effective dielectric constant (K_{eff}) of the Al_2O_3 gate insulator formed by ALD is ~ 9.0 . The radius (r) of ZnO nanowire located in the channel area of the device, which was verified by FE-SEM in the inset of Fig. 3(a), is ~ 15 nm and the channel length (L) between source drains is ~ 5.0 μ m. From these values, the field effect mobility (μ_{eff}) was calculated as ~ 41.32 $cm^2/V\cdot s$. In previous studies, ZnO nanowire transistors were found to have an I_{on}/I_{off} ratio of 10^5 - 10^7 and $\mu_{eff} \sim 3$ - 75 $cm^2/V\cdot s$.³⁷⁻³⁹ Compared with these established results, our top gate-structural nanowire transistor made of ZnO nanowires grown on MGF is comparable in performance.

In summary, this study has verified that ZnO nanowire can be grown directly on MGF without a metal catalyst with

remarkable control of nanowire location. MGFs can be easily patterned through conventional photolithography and O_2 plasma etching to create areas for nanowire growth. In addition, it could be used in its original patterned shape without transformation, similar to the aggregation of metal seeds, even at the nanowire-growing temperature using the CVD. The growth of nanowire in the horizontal direction was readily achieved, as nanowires were grown not only on top of the MGFs but also on the exposed side of MGFs covered with a capping layer. MGFs were patterned with features of desired sizes at intended locations and used as seed material to grow ZnO nanowires directly on the substrate. By utilizing these grown nanowires as a channel, a top-gate structural nanowire transistor was fully fabricated. The characteristics of the ZnO nanowire transistor are comparable to those fabricated in previous studies. Therefore, we have developed a valuable method for aligning nanowires at desired locations via a bottom-up approach for the fabrication of nanowire-based devices.

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- ¹E. H. Hwang, S. Adam, and S. Das Sarma, *Phys. Rev. Lett.* **98**, 186880 (2007).
- ²S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Özyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima, *Nat. Nanotechnol.* **5**, 574 (2010).
- ³X. Wang, L. Zhi, and K. Mullen, *Nano Lett.* **8**, 323 (2008).
- ⁴J. Wu, M. Agrawal, H. A. Becerril, Z. Bao, Z. Liu, Y. Chen, and P. Peumans, *ACS Nano* **4**, 43 (2010).
- ⁵B. Huang, Z. Li, Z. Liu, G. Zhou, S. Hao, J. Wu, B.-L. Gu, and W. Duan, *J. Phys. Chem. C* **112**, 13442 (2008).
- ⁶A. K. Geim, *Science* **324**, 1530 (2009).
- ⁷Y. Cui and C. M. Lieber, *Science* **291**, 851 (2001).
- ⁸S. Ju, J. Li, J. Liu, P.-C. Chen, Y. Ha, F. Ishikawa, H. Chang, C. Zhou, A. Facchetti, D. B. Janes, and T. J. Marks, *Nano Lett.* **8**, 997 (2008).
- ⁹T. Toriyama, D. Funai, and S. Sugiyama, *J. Appl. Phys.* **93**, 561 (2003).
- ¹⁰J. K. W. Yang, E. Dauler, A. Ferri, A. Pearlman, A. Verevkin, G. Gol'tsman, B. Voronov, R. Sobolewski, W. E. Keicher, and K. K. Berggren, *IEEE Trans. Appl. Supercond.* **15**, 626 (2005).
- ¹¹Y. Sun, H. Y. Yu, N. Singh, N. S. Shen, G. Q. Lo, and D. L. Kwong, *IEEE Electron Device Lett.* **31**, 390 (2010).
- ¹²J. Bai, X. Duan, and Y. Huang, *Nano Lett.* **9**, 2083 (2009).
- ¹³L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, *Nature* **467**, 305 (2010).
- ¹⁴T. Cohen-Karni, Q. Qing, Q. Li, Y. Fang, and C. M. Lieber, *Nano Lett.* **10**, 1098 (2010).
- ¹⁵A. C. Ferrari, *Solid State Commun.* **143**, 47 (2007).
- ¹⁶L. M. Malard, M. A. Pimenta, G. Dresselhaus, and M. S. Dresselhaus, *Phys. Rep.* **473**, 51 (2009).
- ¹⁷A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, and A. K. Geim, *Phys. Rev. Lett.* **97**, 187401 (2006).
- ¹⁸A. Gupta, G. Chen, P. Joshi, S. Tadigadapa, and P. C. Eklund, *Nano Lett.* **6**, 2667 (2006).
- ¹⁹S. Lee, K. Lee, and Z. H. Zhong, *Nano Lett.* **10**, 4702 (2010).
- ²⁰A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, *Nano Lett.* **9**, 30 (2009).
- ²¹C. Geng, Y. Jiang, Y. Yao, X. Meng, J. A. Zapien, C. S. Lee, Y. Lifshitz, and S. T. Lee, *Adv. Funct. Mater.* **14**, 589 (2004).
- ²²W. I. Park, D. H. Kim, S.-W. Jung, and G.-C. Yi, *Appl. Phys. Lett.* **80**, 4232 (2002).
- ²³L. E. Greene, M. Law, J. Goldberger, F. Kim, J. C. Johnson, Y. Zhang, R. J. Saykally, and P. Yang, *Angew. Chem. Int. Ed.* **42**, 3031 (2003).
- ²⁴M. Guo, P. Diaio, and S. Cai, *J. Sol. State Chem.* **178**, 1864 (2005).

- ²⁵J. W. P. Hsu, D. R. Tallant, R. L. Simpson, N. A. Missert, and R. G. Copeland, *Appl. Phys. Lett.* **88**, 252103 (2006).
- ²⁶B. Mand, J. Stang, T. Mårtensson, A. Mikkelsen, J. Eriksson, L. S. Karlsson, G. Bauer, L. Samuelson, and W. Seifert, *Nano Lett.* **6**, 1817 (2006).
- ²⁷J. S. Jeong and J. Y. Lee, *Nanotechnology* **21**, 475603 (2010).
- ²⁸S. T. Pantelides, *Deep Centers in Semiconductors* (Gordon and Breach, New York, 1986).
- ²⁹S. J. Henley, M. N. R. Ashfold, D. P. Nicholls, P. Wheatley, and D. Cherns, *Appl. Phys. A* **79**, 1169 (2004).
- ³⁰N. Wang, Y. H. Tang, Y. F. Zhang, C. S. Lee, and S. T. Lee, *Phys. Rev. B* **58**, 16024 (1998).
- ³¹Y.-J. Kim, J.-H. Lee, and G.-C. Yi, *Appl. Phys. Lett.* **95**, 213101 (2009).
- ³²D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan, and K. C. Saraswat, *Appl. Phys. Lett.* **83**, 2432 (2003).
- ³³S. Ju, A. Facchetti, Y. Xuan, J. Liu, F. Ishikawa, P. Ye, C. Zhou, T. J. Marks, and D. B. Janes, *Nat. Nanotechnol.* **2**, 378 (2007).
- ³⁴E. N. Dattoli, Q. Wan, W. Guo, Y. Chen, X. Pan, and W. Lu, *Nano Lett.* **7**, 2463 (2007).
- ³⁵S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
- ³⁶S. Ramo, J. R. Whinnery, and T. V. Duzer, *Fields and Waves in Communication Electronics* (Wiley, New York, 1994).
- ³⁷J. Goldberger, D. J. Sirbuly, M. Law, and P. Yang, *J. Phys. Chem. B* **109**, 9 (2005).
- ³⁸W. I. Park, J. S. Kim, G.-C. Yi, M. H. Bae, and H.-J. Lee, *Appl. Phys. Lett.* **85**, 5052 (2004).
- ³⁹Y. W. Heo, L. C. Tien, Y. Kwon, D. P. Norton, S. J. Pearton, B. S. Kang, and F. Ren, *Appl. Phys. Lett.* **85**, 2274 (2004).